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Ali Makoui

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Patent Application for:

Steven Teig, et al.

Serial No.: 10/079,270

Filing Date: 02/20/2002

For: METHOD AND APPARATUS FOR COMPUTING PLACEMENT COSTS

Examiner: Paul Dinh

Group Art Unit: 2825

APPEAL BRIEF

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This is an Appeal from the final rejection of claims 1-18 in the above-referenced application. In accordance with 37 C.F.R. § 41.37, this Appeal Brief, along with the accompanying Appendix, is accompanied by the required fee. Please charge any additional fees or credit any overpayment to Deposit Account No. **50-1128**.

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Client Docket: 2002 077 P05
Attorney Docket: SPLX.P0127
PTO Serial Number: 10/079,270

I. REAL PARTY IN INTEREST

The real party in interest to this Appeal is Cadence Design Systems, a Delaware Corporation, having its principal place of business in San Jose, California.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences known to the Appellants, the Appellants' legal representative, or assignees thereof.

III. STATUS OF CLAIMS

Claims 1-18 are pending in the present application. The Examiner has rejected claims 1-18.

IV. STATUS OF AMENDMENTS

No amendments to the application were submitted after final rejection.

V. SUMMARY OF CLAIMED SUBJECT MATTER

A. Independent Claim 1

Claim 1 recites a method of placing a set of circuit elements in the circuit layout for a placer that partitions a region of a circuit layout into several sub-regions. *See e.g., Specification, page 34, line 20 to page 35, line 1.* This method identifies during a placement operation, for a set of sub-regions that contain the circuit elements, a connection graph that connects the set of sub-regions. *See e.g., Specification, page 36, lines 10-19.* The connection graph has at least one edge that is at least partially diagonal. *See e.g., Specification, page 36, lines 18-19.* The method identifies a placement cost from an attribute of the connection graph. *See e.g., Specification, page 37, lines 13-19.* The placement cost specifies a cost for the placement of the circuit elements. *See e.g., Specification,*

page 37, lines 16-19. The method uses the placement cost, during a placement operation, to identify a placement for the circuit elements. *See e.g., Specification, page 37, line 20 to page 38, line 7.* The placement specifies positions in the circuit layout for the circuit elements. *See e.g., Specification, page 35, lines 17-21.*

B. Independent Claim 10

Claim 10 recites a computer readable medium that stores a program for placing a set of circuit elements in the circuit layout. This computer program is for a placer that partitions a region of a circuit layout into several sub-regions. *See e.g., Specification, page 34, line 20 to page 35, line 1.* The computer program has a first set of instructions for identifying during a placement operation, for a set of sub-regions that contain the circuit elements, a connection graph that connects the set of sub-regions. *See e.g., Specification, page 36, lines 10-19.* The connection graph has at least one edge that is at least partially diagonal. *See e.g., Specification, page 36, lines 18-19.* The computer program has a second set of instructions for identifying a placement cost from an attribute of the connection graph. *See e.g., Specification, page 37, lines 16-19.* The placement cost specifies a cost for the placement of the circuit elements. *See e.g., Specification, page 37, line 20 to page 38, line 7.* The computer program has a third set of instructions for using the placement cost, during a placement operation, to define a position in the in the circuit layout for the circuit elements. *See e.g., Specification, page 35, lines 17-21*

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

I. The Examiner rejected the appealed claims under 35 U.S.C. § 103(a) as being obvious over United States Patent 6,067,409, issued to Scepanovic ("Scepanovic") in view of United States Patent 5,822,214, issued to Rostoker ("Rostoker").

VII. ARGUMENT

The Examiner erred in rejecting the claimed invention by misapplying standards under 35 U.S.C. § 103(a).

A. CLAIMS 1-18 ARE PATENTABLE UNDER 35 U.S.C. § 103 OVER SCEPANOVIC IN VIEW OF ROSTOKER.

In rejecting claims 1-18, the Examiner stated the following:

> Scepanovic discloses substantially all the elements in claims 1 and 10 except "the connection graph has at least one edge that is at least partially diagonal."
>
> Rostoker discloses diagonal connection graph/edge in, i.e., one or more of: col 59 lines 13-65 (Steiner graph/tree for thee dimensional routing), fig 8, 43, 73-74.
>
> *(Office Action mailed 02/24/05, page 3, Section 5)*

It is the burden of the Examiner to establish a prima facie case of obviousness when rejecting claims under 35 U.S.C. §103. In re Piasecki, 754 F.2D 1468, 223 USPQ 758 (Fed. Cir. 1985). To establish a prima facie case of obviousness, the prior art reference (or references when combined) must teach or suggest all the claim limitations. In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

In this case, Appellants respectfully submit that the Examiner has not established the prima facie case of obviousness, as the suggested combination of the references does not teach or suggest

all the claim limitations. Specifically, Appellants respectfully submit that the cited combination of references does not disclose, teach, or suggest a method that identifies during a placement operation, for a set of sub-regions that contain the circuit elements, a connection graph that connects the set of sub-regions, where the connection graph has at least one edge that is at least partially diagonal.

Moreover, the mere fact that references can be combined or modified does not render the resultant combination obvious, unless the prior art also suggests the desirability of the combination. In re Kotzab, 217 F.3d 1365, 1371, 55 USPQ2d 1313, 1318 (Fed. Cir. 2000). It is improper to use the inventor's disclosure as a road map for selecting and combining prior art disclosures. Grain Processing Corp. v. American Maize-Products Corp., 840 F.2d 902, 907 (Fed. Cir. 1988). Absent such a showing in the prior art, the Examiner has impermissibly used "hindsight" by using the Appellants' teaching as a blueprint to hunt through the prior art for the claimed elements and combine them as claimed. In re Zuko, 111 F.3d 887, 42 USPQ2d 1476 (Fed. Cir. 1997).

As further described in below, the Examiner's rejection has relied on impermissible piecemeal, hindsight combination of features from different references. This hindsight, piecemeal reconstruction is specifically problematic as the Examiner has not identified any proper suggestions or motivations in the art for establishing this combination.

1. **THE SUGGESTED COMBINATION OF THE CITED REFERENCES DOES NOT TEACH, SUGGEST OR DISCLOSE IDENTIFYING DURING A PLACEMENT OPERATION, A CONNECTION GRAPH THAT CONNECTS THE SET OF SUB-REGIONS, WHERE THE CONNECTION GRAPH HAS AT LEAST ONE EDGE THAT IS AT LEAST PARTIALLY DIAGONAL**

Appellants respectfully submit that the combination of Scepanovic and Rostoker does not

disclose teach, or even suggest all the claim limitations. Scepanovic describes a method that places cells by computing a cost for improving cell placement. Scepanovic computes this cost for improving cell placement by only considering vertical and horizontal routes. *See* Scepanovic, column 43, lines 34-50. Therefore, Scepanovic does not describe a method that identifies, during a placement operation, a connection graph that connects the set of sub-regions, where the connection graph has at least one edge that is at least partially diagonal.

The Examiner states that Rostoker discloses such a connection graph that has at least one edge that is at least partially diagonal. However, Rostoker describes diagonal routes used during a routing operation. *See Rostoker, column 58, lines 23-35.* First, Rostoker's routes are not edges of a connection graph. Second, in contrast to the claims, these diagonal routes are not identified during a placement operation. Third, placement and routing operations are two different types of operations. *See specification, page 2, line 23 to page 3, line 6.* Therefore, Appellants respectfully submit that the combination of Scepanovic and Rostoker does not disclose, teach or even suggest a method that identifies, during a placement operation, a connection graph that connects a set of sub-regions, where the connection graph has at least one edge that is at least partially diagonal.

2. THE EXAMINER REJECTED THE CLAIMS BY RELYING ON IMPERMISSIBLE PIECEMEAL, HINDSIGHT COMBINATION OF REFERENCES.

Appellants respectfully submit that the Examiner has not identified any proper suggestion or motivation in the art for combining the cited references. Without the identification of a proper suggestion or motivation to combine the cited references, the Examiner has not met his *prima facie* case of obviousness. As previously mentioned, Scepanovic describes placement operations, whereas Rostoker describes using diagonal routes during routing operations. As mentioned above, placement and routing operations are completely different types of operations in the design of an integrated

circuit. *See specification, page 2, line 23 to page 3, line 6.*

The cited references, therefore, do not suggest the desirability of the combination and the Examiner has impermissibly used hindsight by using Appellants' own claims as a template for combining features from different references for the claimed elements. The only motivation the Examiner has offered is that "it would have obvious to one of ordinary skill in the art at the time of the invention to utilize [a] 'connection graph [that] has at least one edge that is at least partially diagonal' because diagonal connection graph or diagonal routing graph reduces/shortens/minimizes routing distances, wire lengths, path lengths, interconnect paths." *See Office Action May 5, 2005, page 3.*

The prior art can be modified or combined to reject claims as *prima facie* as long as there is a reasonable expectation of success. *In re Merck & Co., Inc.*, 8000 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Appellants respectfully submit there is no reasonable expectation of success in the combination of the cited references. In this case, Scepanovic describes placement operations and Rostoker describes using diagonal routes during routing operations. As mentioned above placement and routing operations are completely different processes of an IC design process. Therefore, there is no reasonable expectation of success that Rostoker's diagonal routes used during routing operations can be implemented in Scepanovic's placement operations. Therefore, the Examiner has not met the burden of establishing a *prima facie* case of why it makes sense to combine these references.

VIII. CLAIMS APPENDIX

See attached Appendix A.

IX. EVIDENCE APPENDIX

In this Appeal Brief, Appellants have not provided an Evidence Appendix.

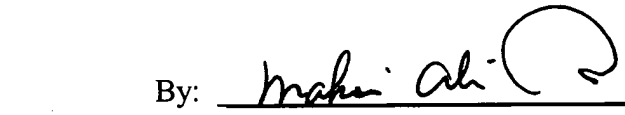
X. RELATED PROCEEDINGS APPENDIX

There are no related appeals or interferences known to the Appellants, the Appellants' legal representative, or assignees thereof.

XI. CONCLUSION

In view of the foregoing, Appellants respectfully submit that the claims are patentable. Appellants hereby request that the Board overturn the Examiner's finding that the claims are unpatentable under 35 U.S.C. § 103(a).

Respectfully submitted,

Dated: January 11, 2006 By: 

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APPENDIX A

The following claims are the subject of this Appeal.

1. For a placer that partitions a region of a circuit layout into a plurality of sub-regions, a method of placing a set of circuit elements in the circuit layout, the method comprising:

a) for a set of sub-regions that contain the circuit elements, identifying a connection graph during a placement operation that connects the set of sub-regions, wherein the connection graph has at least one edge that is at least partially diagonal;

b) identifying a placement cost from an attribute of the connection graph, wherein the placement cost specifies a cost for the placement of the circuit elements; and

c) using the placement cost during a placement operation to identify a placement for the circuit elements, wherein the placement specifies positions in the circuit layout for the circuit elements.

2. The method of claim 1, wherein the attribute is a length of the connection graph, and the placement cost equals the length of the connection graph.

3. The method of claim 2, wherein the length of the connection graph provides an estimate of a length of a route for routing a net that is defined to include the circuit elements in the set of sub-regions.

4. The method of claim 2, wherein a net is defined to include the set of circuit elements in the circuit-layout region, the method further comprising:

before the identification of the connection graph, identifying the set of sub-regions as the set that contains the set of circuit elements of the net.

5. The method of claim 4 further comprising:

from a storage structure, retrieving the attribute based on the identity of the set

of sub-regions.

6. The method of claim 4, wherein the circuit layout region comprises a set of nets, wherein each net is defined to include a set of circuit elements, the method further comprising:

for each net in the circuit-layout region,

(i) identifying a set of sub-regions that contains the set of circuit elements of the net;

(ii) identifying a connection graph that connects the set of sub-regions;

(iii) identifying the length of the connection graph;

wherein some connection graphs have at least one edge that is at least partially diagonal;

identifying an overall placement cost from the identified length of each connection graph.

7. The method of claim 6, wherein the overall placement cost quantifies the quality of an initial placement configuration.

8. The method of claim 7, wherein the placer works in conjunction with a router that uses a wiring model that allows routing in at least one diagonal direction, wherein the initial placement configuration is specified by a placer that does not account for potential diagonal wiring during routing.

9. The method of claim 1, wherein the connection graph is a Steiner tree.

10. For a placer that partitions a region of a circuit layout into a plurality of sub-regions, a computer readable medium that stores a program for placing a set of circuit elements in the circuit layout, the program comprising:

a) a first set of instructions for identifying during a placement operation, for a set

of sub-regions that contain the circuit elements, a connection graph that connects the set of sub-regions, wherein the connection graph has at least one edge that is at least partially diagonal;

b) a second set of instructions for identifying a placement cost from an attribute of the connection graph, wherein the placement cost specifies a cost for the placement of the circuit elements; and

c) a third set of instructions for using the placement cost during a placement operation to define a position in the circuit layout for the circuit elements.

11. The computer readable medium of claim 10, wherein the attribute is a length of the connection graph, and the placement cost equals the length of the connection graph.

12. The computer readable medium of claim 11, wherein the length of the connection graph provides an estimate of a length of a route for routing a net that is defined to include the circuit elements in the set of sub-regions.

13. The computer readable medium of claim 11, wherein a net is defined to include the set of circuit elements in the circuit-layout region, the computer program further comprising:

a third set of instructions for identifying, before the identification of the connection graph, the set of sub-regions as the set that contains the set of circuit elements of the net.

14. The computer readable medium of claim 13, wherein the computer program further comprises:

a fourth set of instructions for retrieving, from a storage structure, the attribute based on the identity of the set of sub-regions.

15. The computer readable medium of claim 13, wherein the circuit layout region comprises a set of nets, wherein each net is defined to include a set of circuit elements, the computer program further comprising:

for each net in the circuit-layout region,

(i) a fourth set of instructions for identifying a set of sub-regions that contains the set of circuit elements of the net;

(ii) a fifth set of instructions for identifying a connection graph that connects the set of sub-regions;

(iii) a sixth set of instructions for identifying the length of the connection graph;

wherein some connection graphs have at least one edge that is at least partially diagonal;

a seventh set of instructions for identifying an overall placement cost from the identified length of each connection graph.

16. The computer readable medium of claim 15, wherein the overall placement cost quantifies the quality of an initial placement configuration.

17. The computer readable medium of claim 16, wherein the placer works in conjunction with a router that uses a wiring model that allows routing in at least one diagonal direction, wherein the initial placement configuration is specified by a placer that does not account for potential diagonal wiring during routing.

18. The computer readable medium of claim 10, wherein the connection graph is a Steiner tree.